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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

WEINMAN, SEAN M

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/633,360

Applicant(s)

FLAUTNER, KRISZTIAN

Examiner

Sean Weinman

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-66 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-66 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/11/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claims 1-66 are presented for examination.

Claim Objections

Claim 61 is objected to because of the following informalities:

Claim 61 recites, "operating at different clock speeds and are provided with different supply voltage levels". Claim 59, from which it depends, does not mention a "supply voltage level", whereas claim 60 recites "a supply voltage level". It is believed that claim 61 was intended to be depend from claim 60 and has been treated as such for the remainder of this Office action.

Appropriate clarification and/or correction are required in response to this Office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 15, 21, 22, 37, 43, 44, 59, 65 and 66 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites "a clock speed" on line 3. It is unclear whether this is intended to be the same as or different from the "clock speed" recited in claim 1 line 7.

Claim 21 recites "a clock speed" on line 3. It is unclear whether this is intended to be the same as or different from the "clock speed" recited in claim 1 line 7.

Claim 22 recites “a level of parallelism” on line 3. It is unclear whether this is intended to be the same as or different from the “potential level of parallelism” recited in claim 18 line 2.

Claim 37 recites “ a clock speed” on line 3. It is unclear whether this is intended to be the same as or different from the “clock speed” recited in claim 23 line 7.

Claim 43 recites “a clock speed” on line 3. It is unclear whether this is intended to be the same as or different from the “clock speed” recited in claim 23 line 7.

Claim 44 recites “a level of parallelism” on line 3. It is unclear whether this is intended to be the same as or different from the “potential level of parallelism” recited in claim 40 line 2.

Claim 59 recites “a clock speed” on line 3. It is unclear whether this is intended to be the same as or different from the “clock speed” recited in claim 45 line 7.

Claim 65 recites “a clock speed” on line 3. It is unclear whether this is intended to be the same as or different from the “clock speed” recited in claim 45 line 7.

Claim 66 recites “a level of parallelism” on line 3. It is unclear whether this is intended to be the same as or different from the “potential level of parallelism” recited in claim 62 line 2.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14, 16-17, 19-20, 23-36, 38-39, 41-42, 45-58, 60-61, 63-64 are rejected under 35 U.S.C. 102(b) as being anticipated by Nicol et al. (US Patent No. 6,141,762).

As per claim 1, Nicol et al. teaches the invention comprising:

a plurality of processors (Col. 2 lines 50-53) operable to execute respective streams of program instructions (Col. 3 lines 10-21), said respective streams of program instructions being separate processing threads within a multi-processing environment (Col. 3 lines 10-21); and a clock speed controller operable to select one of a plurality of different non-zero clock speeds as a clock signal controlling execution of program instructions by at least one of said processors (Col. 3 lines 22-30 and 66-67 and Col. 4 lines 1-6 and 17-21 Nicol et al. does not expressly detail a clock speed controller or clock signal. However, it is readily recognized that a clock speed controller and clock signal are needed to adjust the clock frequency.), whereby said clock speed may be reduced by said clock speed controller to reduce energy consumption of said apparatus in accordance with a required processing rate of said apparatus (Col. 3 lines 22-30 and 66-67 and Col. 4 lines 1-6 and 11-13 Col. 5 lines 23-28).

As per claim 2, Nicol et al. teaches the invention comprising:

wherein said clock speed controller is operable to dynamically select said clock signal to have a desired clock speed (Col. 3 lines 22-30 and 66-67 and Col. 4 lines 1-6 and 11-13).

As per claim 3, Nicol et al. teaches the invention comprising:

wherein said clock speed controller is responsive to a detected level of parallelism between respective streams of program instructions to dynamically select said clock signal (Col. 3 lines 10-21 and Col. 5 lines 23-28).

As per claim 4, Nicol et al. teaches the invention comprising:

comprising a parallelism detector being one of: a hardware circuit detecting parallel processing activity of said plurality of processors; and one of said processors executing a parallelism detecting algorithm (Col. 3 lines 10-21 and 22-30 and 66-67 and Col. 4 lines 1-6 and 11-13 and Col. 5 lines 23-28 Nicol et al. does not expressly detail a parallelism detecting algorithm. However, it is readily recognized that a parallelism detecting algorithm is needed for the operating system to maximize the parallelism.)

As per claim 5, Nicol et al. teaches the invention comprising:

wherein said clock speed controller is responsive to a detected level of thread level parallelism (Col. 3 lines 10-21 and 22-30 and 66-67 and Col. 4 lines 1-6 and Col. 5 lines 23-28).

As per claim 6, Nicol et al. teaches the invention comprising:

said detected level of thread level parallelism includes parallelism between independent processes and parallelism within a single process (Col. 3 lines 10-21 and 66-67 and Col. 4 lines 1-6 and Col. 5 lines 23-28).

As per claim 7, Nicol et al. teaches the invention comprising:

wherein said thread level parallelism is a measure of how many parallel threads are executing for periods when at least one thread is executing (Col. 3 lines 10-21 and 66-67 and Col. 4 lines 1-6 and Col. 5 lines 23-28).

As per claim 8, Nicol et al. teaches the invention comprising:

wherein said plurality of processors are operable to execute respective streams of program instructions under control of a respective clock signal having a plurality of different clock speeds (Col. 3 lines 22-30 and 66-67 and Col. 4 lines 1-6 and 17-21).

As per claim 9, Nicol et al. teaches the invention comprising:

said plurality of processors share a common clock speed and a common clock source (Col. 4 lines 17-37).

As per claim 10, Nicol et al. teaches the invention comprising:

wherein said plurality of processors have independently adjustable clock speeds (Col. 5 lines 66-67 and Col. 6 lines 1-2).

As per claim 11, Nicol et al. teaches the invention comprising:

said plurality of processors are formed on a single integrated circuit (Col. 2 lines 50-53).

As per claim 12, Nicol et al. teaches the invention comprising:

wherein said clock speed controller comprises at least one of said processors executing a clock speed controlling algorithm (Col. 3 lines 66-67 and Col. 4 lines 1-6 Nicol et al. does not expressly detail a clock speed controller algorithm. However, it is readily recognized that a clock speed controller algorithm is needed for the operating system to adjust the clock frequency.).

As per claim 13, Nicol et al. teaches the invention comprising:

wherein said clock speed controlling algorithm is part of an operating system kernel (Col. 3 lines 66-67 and Col. 4 lines 1-6).

As per claim 14, Nicol et al. teaches the invention comprising:

wherein said operating system kernel is distributed between said plurality of processors (Col. 3 lines 66-67 and Col. 4 lines 1-6).

As per claim 16, Nicol et al. teaches the invention comprising:

wherein said clock speed controller is also operable to control a supply voltage level for said at least one processor such that said supply voltage level is reduced as said clock speed is reduced (Col. 3 lines 66-67 and Col. 4 lines 1-6 and 11-13).

As per claim 17, Nicol et al. teaches the invention comprising:

wherein said clock speed controller is operable such that processors operating at different clock speeds are provided with different supply voltage levels (Col. 5 lines 66-67 and Col. 6 lines 1-2).

As per claim 19, Nicol et al. teaches the invention comprising:

wherein said plurality of processors are a plurality of general purpose processor cores (Col. 2 lines 50-53).

As per claim 20, Nicol et al. teaches the invention comprising:

wherein said plurality of processors include at least one of: a general purpose processor; a reconfigurable processor; a hardware accelerator engine; an application specific processor; and a digital signal processor (Col. 2 lines 50-53 It is obvious to one of ordinary skill in the art that the processors are general purpose and digital signal processors).

As per claims 23-44, it is directed to the method of processing data as set forth in claims 1-22. Since Nicol et al. teach the claimed data processing apparatus, Nicol et al. teach the method for operating the claimed data processing apparatus.

As per claims 45-66, it is directed to the computer program operable to control a plurality of processors as set forth in claims 1-22. Since Nicol et al. teach the claimed data processing apparatus, Nicol et al. teach the computer program operable to control the claimed data processing apparatus.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 15, 18, 21-22, 37, 40, 43-44, 59, 62, and 65-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nicol et al. (US Patent No. 6,141,762) in further view of Beard (US Patent No. 5,627,412).

As per claim 15, Nicol et al. teaches a data processing apparatus containing a plurality of processors to execute streams of program instructions and a clock speed controller to select clock speeds in accordance with the required processing rate of the instructions for all of the reasons stated above. However, Nicol et al. fails to detail that the apparatus has a maximum processing workload and when the operating below that workload the controller selects a clock speed less than a maximum clock speed for the processor.

Beard teaches a power system that controls the clock frequency and supply voltage based on the demand of certain program instructions.

wherein said apparatus has a maximum required processing workload and when operating below said maximum required processing workload said clock speed controller selects a clock speed less than a maximum clock speed for said at least one processor (Col. 3 lines 66-67 and Col. 4 lines 1-12).

Beard teaches that the clock frequency and supply voltage may be altered based on the requirements of the program instructions. If a program instruction does not meet the maximum processing workload then a clock frequency and supply voltage less than maximum will be demanded.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Nicol et al. and Beard because they both teach systems which control the clock frequency and supply voltage of a processor based on the requirements to process the program instructions.

As per claim 18, Beard teaches the invention comprising:

wherein said clock speed controller is responsive to a determination of a potential level of parallelism above a threshold level of parallelism to wake a processor from a sleep mode into a clock mode such that said processor may execute a parallel stream of program instructions (Col. 3 lines 66-67 and Col. 4 lines 1-12 In response to the determination of the level of parallelism, which is based on the demand of processing speed and power of the program instruction, the processor will awake from a low power

mode to a required clock frequency and supply voltage to process the program instructions.)

As per claim 21, Beard teaches the invention comprising:

wherein said clock speed controller is operable to reduce a clock speed of at least one processor when said detected level of parallelism has fallen below a threshold level for more than a threshold amount of time (Col. 3 lines 66-67 and Col. 4 lines 1-12 In response to the determination of the level of parallelism, which is based on the demand of processing speed and power of the program instruction, the processor will fall into a low power mode with a low clock frequency and low supply voltage.)

As per claim 22, Beard teaches the invention comprising:

wherein said clock speed controller is operable to speculatively wake said processor from said sleep mode to determine a level of parallelism that may be achieved (Col. 3 lines 66-67 and Col. 4 lines 1-12 In response to the determination of the level of parallelism, which is based on the demand of processing speed and power of the program instruction, the processor will awake from a low power mode to a required clock frequency and supply voltage to process the program instructions.)

As per claims 37, 40, and 43-44, it is directed to the method of processing data as set forth in claims 15, 18, and 21-22. Since Nicol et al. teach the claimed data processing apparatus, Nicol et al. teach the method for operating the claimed data processing apparatus.

As per claims 59, 62, and 65-66, it is directed to the computer program operable to control a plurality of processors as set forth in claims 15, 18, and 21-22. Since Nicol

et al. teach the claimed data processing apparatus, Nicol et al. teach the computer program operable to control the claimed data processing apparatus.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sean Weinman
Examiner
Art Unit 2115



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PRIMARY EXAMINER